REMARKS

Claims 1-18 are pending in the application. In the Office Action, Claims 1-2 and 6 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pub. No. 2004/0120411 of Walton et al. in view of U.S. Pub. No. 2003/0086479 of Naguib; and Claims 3-5 and 7-18 were found to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Examiner's finding of allowable subject matter in Claims 3-5 and 7-18 is gratefully acknowledged.

Claim 1, which is the only rejected independent claim, was rejected over the combination of Walton et al. and Naguib.

Walton et al. discloses closed-loop rate control for data transmission on multiple parallel channels. An inner loop estimates the channel conditions for a communication link and selects a suitable data rate for each of the multiple parallel channels based on the channel estimates. For each parallel channel, a received SNR is computed based on the channel estimates, an operating SNR is computed based on the received SNR and an SNR offset for the parallel channel, and the data rate is selected based on the operating SNR for the parallel channel and a set of required SNRs for a set of data rates supported by the system. (See Abstract of Walton et al.).

Regarding independent Claim 1, the Examiner states that Walton et al. discloses all of the elements of Claim 1 except for "a parallel-to-serial converter for sequentially arranging and outputting the two symbols detected by each of the first and second decoders." It is respectfully submitted that the Office Action misconstrues Walton et al. First, Fig. 11, element 1132a and page 14 [0191] of Walton et al. are cited for teaching "a symbol demapper for receiving signals transmitted from four antennas to at least one receiving antenna during four time intervals." Then, the Examiner commented that a symbol demapper is functionally equivalent to the claimed symbol arranger. However, the cited passage reads as follows:

> RX data processor 964 receives the N_c recovered symbol streams from RX spatial processor 962. Each recovered symbol stream is provided to a respective symbol demapping unit 1132, which demodulates the recovered symbols in accordance with the modulation scheme used for that stream, as indicated by a demodulation control provided by controller 970. The demodulated data stream from each symbol demapping unit 1132 is de-interleaved by an associated channel de-interleaver 1134 in a manner

complementary to that performed at access point 510x for that data stream. (Paragraph 0191.)

From the above passage, it is seen that a demapping unit is functionally a demodulator. To an artisan of ordinary skill in the art, a demodulator converts a analog signal to a digital signal. Unlike Walton et al., the symbol arranger of the present invention, which the Examiner likens to a demodulator, collects signals r_1, r_2, r_3, r_4 received at the receiver antennas. If a single receiver antenna is used, the symbol arranger 330 builds one block from the four received signals r_1, r_2, r_3, r_4. If two or more receiver antennas are used, the symbol arranger 330 builds a block in the form of a matrix from the received signals. In the matrix, the columns correspond to the receiver antennas and the rows correspond to time intervals. (See Specification page 12, lines 2-9.) Therefore, the demapping unit of Walton et al. and the arranger of the present invention are not functionally equivalent, as was alleged in the Office Action.

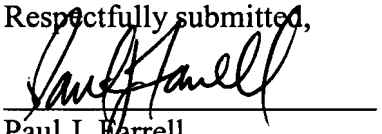
Furthermore, the Examiner cites page 1, paragraph [0010], page 2 [0030-0032], and page 3 paragraph [0038]; page 4 paragraph [0041]; page 10 paragraph [0138] for teaching "wherein the first and second decoders each linearly operate the received signals with the channel gains, pre-detect two symbols using threshold detection, and output the pre-detected two symbols as final symbols if the product of the product of the pre-detected symbols and a constant determined by the channel gains is a minimum." However, after reviewing the cited passages, nowhere does Walton recite a structure that resembles "first and second decoders each linearly operate the received signals with the channel gains." For example, paragraph 0010 makes reference to adjusting the SNR offset for each parallel channel to achieve a target packet error rate (PER) for that parallel channel; paragraph 0038 makes reference to a re-encoded symbol error rate (SER). Accordingly, these rejections are traversed, because the prior art reference fails to teach or suggest all the claim limitations. In order for the Examiner to establish a prima facie case of obviousness, at least the prior art reference must teach or suggest all the claim limitations.

The above noted deficiencies of Walton et al. are not cured by Naguib. As such, independent Claim 1 is believed to be allowable over the combination of Walton et al. and Naguib. Without conceding the patentability *per se*, Claims 2 and 6 are believed to be in condition for allowance at least in view of their dependence from Claim 1.

Accordingly, all of the pending claims, i.e. Claims 1-18, are believed to be in condition

for allowance. If the Examiner believes that a telephone conference or personal interview would facilitate resolution of any remaining matters, it is respectfully requested that the Examiner contact Applicant's attorney at the number given below.

Respectfully submitted,



Paul J. Farrell
Reg. No. 33,494
Attorney for Applicant

THE FARRELL LAW FIRM, P.C.
333 Earle Ovington Blvd.
Uniondale, New York 11553
Tel: (516) 228-3565